High-Frequency Analysis of Embedded Microfluidic Cooling Within 3-D ICs Using a TSV Testbed

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Abstract— **In this paper, the impact of microfluidic cooling on the electrical characteristics of through-silicon vias (TSVs) is investigated for three-dimensional (3-D) integrated circuits (ICs). The design and fabrication of a testbed containing TSVs are presented for two types of heat sinks (micropin-fin and microchannel heat sinks) immersed in deionized (DI) water. The high-frequency characterization of TSVs in the DI water-filled testbed is performed and compared to conventional TSVs in silicon. TSVs in DI water demonstrate higher insertion loss, capacitance, and conductance than TSVs in silicon. In this paper, we also present coaxially shielded TSVs embedded in a pin-fin heat sink and demonstrate the electrical isolation of the signal TSV from the surrounding DI water.**

Keywords-3-D IC; Heat Sink; Microchannel; Micropin-Fin; Microfluidic Cooling; Silicon Interposer; Through-silicon Via.

I. INTRODUCTION

Microfluidic cooling technology has been widely explored as a promising solution for modern integrated circuits (ICs) in which power density has been continuously increasing. In 1981, Tuckerman and Pease introduced an integrated microchannel heat sink in a silicon chip [1]. Since then, many researchers have studied various designs of the microfluidic heat sink to enhance its performance [2]-[5]. Moreover, due to the high cooling capability of microfluidic cooling, there have been efforts to integrate microfluidic cooling with three-dimensional (3-D) ICs, which generally suffer from thermal limits [5]. Micromachined technologies for the integration of microfluidic cooling within 3-D ICs, such as fluidic inlet/outlet (I/O) and electrical microbumps, were demonstrated for die-to-silicon interposer bonding [6]. Moreover, two-tier stacked 3-D IC cooling was demonstrated using tier-independent microfluidic cooling [7].

Recently, the monolithic integration of microfluidic cooling with a field-programmable gate array (FPGA) has been successfully demonstrated [9]. This work highlighted the benefits of a microfluidic-cooled FPGA relative to an air-cooled FPGA; a 60% reduction in junction temperature was shown. This demonstration suggests the feasibility of microfluidic cooling integration for 3-D IC applications. With this trend, there have been various studies to understand the impact of microfluidic cooling on the electrical characteristics of ICs. Due to the high cooling capability of microfluidic cooling, one study reported a 66.2% leakage current reduction in a CMOS chip using microfluidic cooling [10]. In addition, the frequency-dependent electrical characteristics of liquid coolants have been utilized with various passive elements. For example, microfluidic cooling was integrated with an L-band filter to demonstrate a tunable corner frequency of the filter with respect to the dielectric constant of the coolant [11]. A tunable RF sensor with conductor-backed coplanar waveguide (CPW) was integrated to achieve broadband frequency tunability using various coolants: distilled water and a methanol-water solution [12]. In addition, one research study demonstrated the RF isolation of CPW on a liquid crystal polymer substrate from water [13]. However, there remains a need to analyze how liquid cooling impacts the electrical characteristics of interconnects including TSVs. The presence of a coolant between signal and ground interconnects will influence signal propagation including loss, signal integrity, and crosstalk [14].

To address this missing need in the literature, this paper investigates the impact of microfluidic cooling on the electrical characteristics of TSVs, including insertion loss, TSV capacitance, and conductance. Section II discusses the design consideration of a microfluidic cooling testbed containing TSVs using two types of heat sinks. Section III describes the fabrication of two microfluidic heat sinks with embedded TSVs. In Section IV, the high-frequency characterization of microfluidic heat sink-embedded TSVs immersed in deionized (DI) water is reported. Moreover, we evaluate the benefits of coaxially shielded TSVs integrated within microfluidic cooling.

II. DESIGN CONSIDERATION: HIGH-FREQUENCY CHARACTERSTICS OF TSVS WITHIN DI WATER

Figure 1 illustrates a conventional 3-D IC and a 3-D IC with integrated microfluidic cooling. The integration of microfluidic cooling with 3-D ICs enables higher cooling capability to dissipate heat inside the 3D stack. However, in such a liquid-cooled microsystem, the electrical signal propagating through the TSVs may be influenced by the DI water since the TSVs are integrated within the silicon microfluidic heat sink, which is surrounded by DI water.

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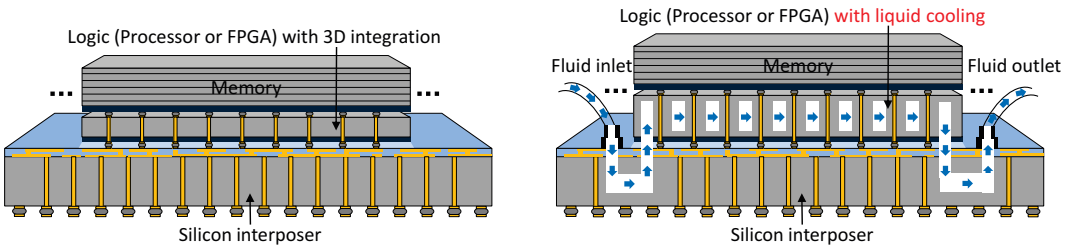


(a) (b)

Fig. 1. (a) Conventional 3D integration with logic (processor or FPGA) and memory on a silicon interposer; multiple stacks can be integrated on an interposer. (b) Envisioned 3D microsystem of logic and memory dice with integrated microfluidic cooling technology on an interposer.

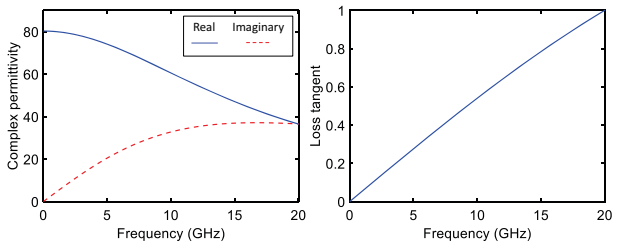
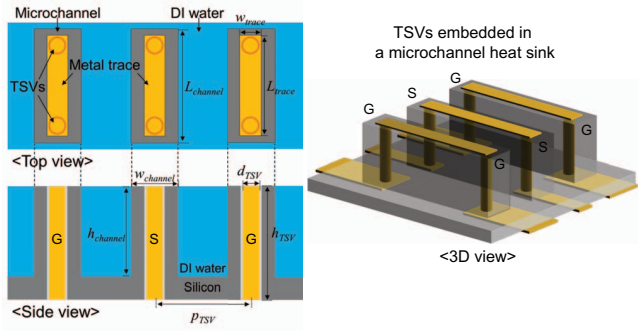


Fig. 2. Real permittivity, imaginary permittivity, and loss tangent of DI water up to 20 GHz [15], [16].



(a)

(b)

Fig. 3. (a) Schematics of ground-signal-ground (GSG) TSVs embedded in a silicon microchannel heat sink. (b) Schematics of TSVs embedded in a silicon micropin-fin heat sink.

The permittivity of DI water significantly varies with respect to frequency, as shown in Fig. 2 [15], [16]. The loss tangent of DI water is relatively high compared to any dielectric material [15], and thus it may induce large attenuation and loss for the TSVs under consideration. Silicon has finite conductivity and a loss tangent of 0.004 at 10 GHz and 25ºC [17]. Figure 3 illustrates a ground-signal-ground (GSG) configuration of TSVs within microfluidic heat sinks. In this configuration, there is a conductive path through silicon and DI water from the signal TSV to the ground TSVs. Thus, it is expected that the conductance and loss of TSVs in DI water will be larger than that of a pure silicon substrate. To analyze the frequency response of TSVs within DI water, this paper presents a testbed containing TSVs (using a GSG TSV configuration) embedded in two types of microfluidic heat sinks: a microchannel-based heat sink (as shown in Fig. 3 (a)) and a micropin-fin based heat sink (as shown in Fig. 3 (b)). The microchannel-embedded TSVs are used for two-port characterization (from the opposite side of the heat sink), while the micropin-fin-embedded TSVs are used for single-port characterization. DI water is filled in the TSV testbed during electrical characterization.

III. Fabrication of Microfluidic Heat Sinks with Embedded TSVs

This section presents the fabrication of TSVs embedded in the two microfluidic heat sinks shown in Figure 3 (microchannel and micropin-fin heat sink). Figure 4 illustrates the fabrication process of the TSVs in microfluidic heat sinks. The fabrication begins with the deposition of silicon dioxide on top of the silicon wafer (Step 1 in Fig. 4), followed by anistropic dry etching of the oxide using a thin chrome mask (Step 2), as shown in Fig. 5. Chrome has a significantly higher selectivity with respect to silicon dioxide (> 50:1). Using the patterned silicon dioxide as an etch mask, the silicon wafer is etched (Step 3) using the high-aspect ratio Bosch process [18]. Etched silicon vias are shown in Fig. 6.

Following the removal of the remaining silicon dioxide after the silicon etch, the wafer is placed into a Tystar furnace for oxide growth to electrically isolate the copper vias from the the silicon substrate. Next, a two-step copper electroplating process (Step 4) is performed to fill the via holes with copper. First, a metal seed layer is deposited on

TABLE I. DIMENSIONS OF TSVS, TRACE, AND MICROFLUIDIC HEAT SINKS

TSV (µm)			Trace (µm)			Heat Sinks[b] (µm)			
d_{TSV}	h_{TSV}	p_{TSV}	w_{trace}	l_{trace}	t_{trace}[a]	d_{pinfin}	h_{pinfin}	$w_{channel}$	$h_{channel}$
13	330	200	20	200	3	75 150	230	75 150	230

[a] Thickness of trace (not presented in Fig. 3).
[b] 'Pinfin' stands for a micropin-fin heat sink, and 'channel' stands for a microchannel heat sink.

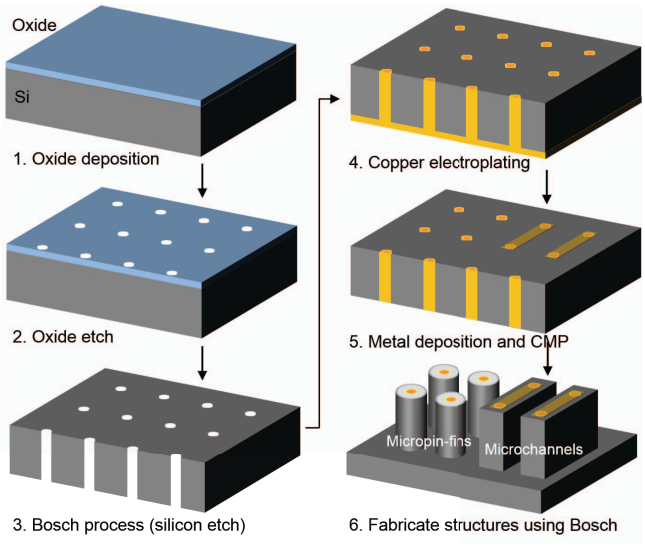


Fig. 4. Fabrication process of TSVs embedded in microfluidic heat sinks (a circular micropin-fin heat sink and a rectangular microchannel heat sink)

the back side of the wafer, and the via holes are closed using DC copper electroplating from the back side of the wafer. Second, a pulsed (duty cycle of 60:40) copper electroplating process is performed using a bottom-up approach from the front side of the wafer. Following electroplating, chemical mechanical polishing (CMP) is performed from both sides of the wafer to remove the over-electroplated copper. Following CMP, the copper traces are selectively deposited using an e-beam evaporator to interconnect TSVs on the back side of the wafer (Step 5). Moreover, to facilitate probing, metal (titanium/copper/gold) pads are deposited on the front side of the wafer, as shown in Fig. 8. Gold passivation is performed on the metal pads to prevent oxidization. Lastly, another Bosch process is performed to fabricate the two types of microfluidic heat sink structures (Step 6) from the back side of the wafer. In this step, the silicon cylindrical and rectangular structures are fabricated for micropin-fins and microchannels, respectively. Figure 7 illustrates SEM images of microchannels with embedded TSVs and metal traces (Fig. 7 (a)) and micropin-fins with embedded TSVs (Fig. 7 (b)). Dimensions of microfluidic heat sinks, TSVs, and metal traces are summarized in Table 1.

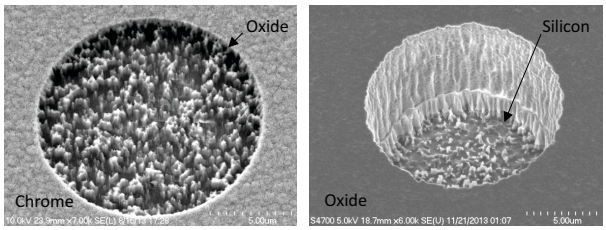


Fig. 5. SEM images of patterned chrome mask for oxide etching (left) and oxide mask for silicon etching (right).

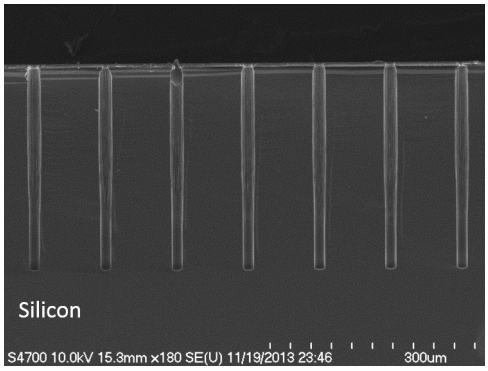
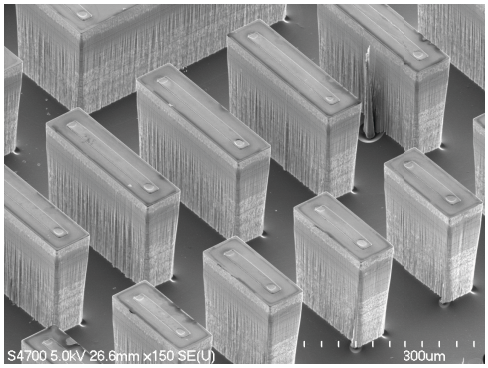
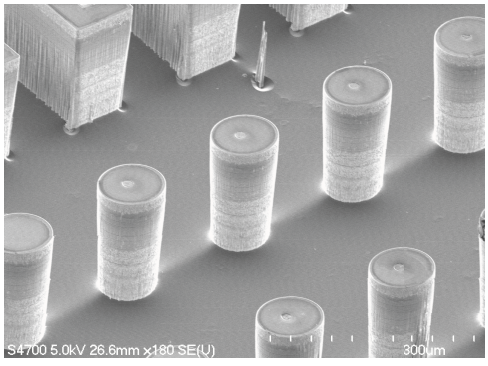


Fig. 6. SEM image of etched silicon vias using the high-aspect ratio Bosch process (cross-sectional view).

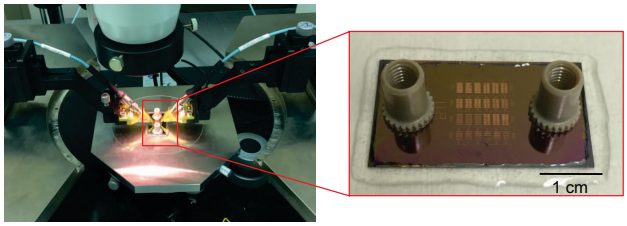


(a)



(b)

Fig. 7. SEM images of silicon microfluidic heat sinks with embedded TSVs. (a) Microchannel heat sink ($w_{channel}$ of 75 µm). (b) Micropin-fin heat sink (d_{pinfin} of 75 µm).



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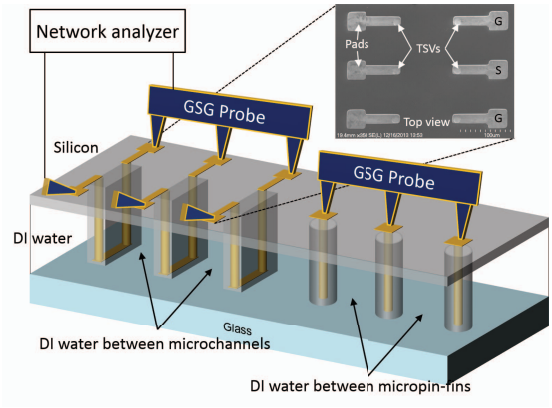


(b)

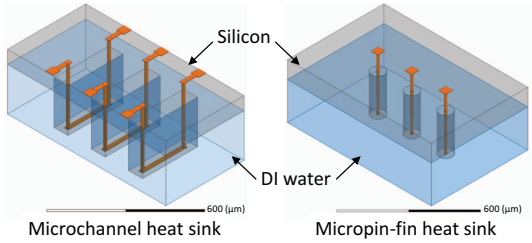
Fig. 8. High-frequency measurement setup of the fabricated testbed: (a) photographs of the setup and testbed, and (b) schematic of the setup. DI water is filled between microchannels during electrical characterization.

IV. High-Frequency Characterization of the TSVs Within DI Water

The fabricated testbed is capped with a glass slide and connected with external fluidic ports for DI water delivery. The high-frequency characterization of the testbed is performed using a microprobe station, Cascade Microtech 200-µm-pitch |Z| probes, and a Keysight network analyzer in the frequency range of 10 MHz to 20 GHz. Figure 8 illustrates the high-frequency measurement setup of TSVs embedded in a microchannel heat sink (left) and a micropin-fin heat sink (right). For the microchannel heat sink-embedded TSVs, two-port characterization is performed to analyze the insertion loss of TSVs while for the micropin-fin heat sink-embedded TSVs, single-port characterization is performed to extract the capacitance and conductance of the TSVs. To validate our measurements, ANSYS High-Frequency Structure Simulator (HFSS) is utilized and compared in Fig. 9. In the simulation, the permittivity and loss tangent of DI water is based on properties from [15], and a DI water layer is created surrounding the microfluidic heat sink, as shown in Fig. 9 (a).

A. Insertion Loss Characterization of TSVs and Traces in a Microchannel Heat Sink

In the microchannel heat sink testbed (the left setup in Fig. 8(b)), each microchannel contains two TSVs, and DI water is filled between the microchannels; there is a capacitive path through the DI water from the signal TSVs



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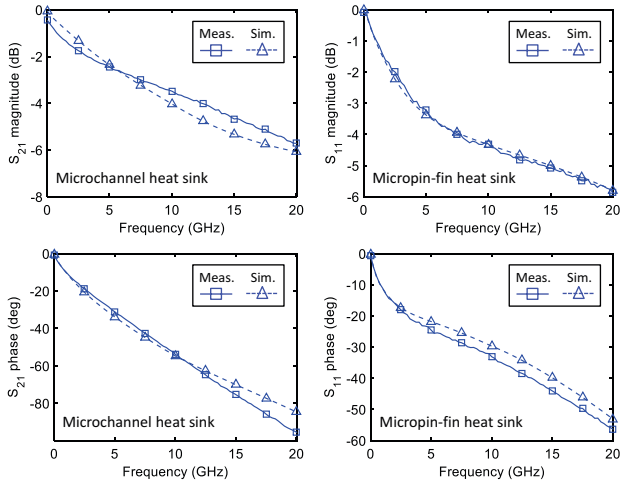

(b)

Fig. 9. (a) Two heat sink structures in HFSS simulation. (b) Comparison between simulations and measurements: S_{21} magnitude and phase for TSVs in a microchannel heat sink with DI water (left), and S_{11} magnitude and phase for TSVs in a micropin-fin heat sink with DI water (right).

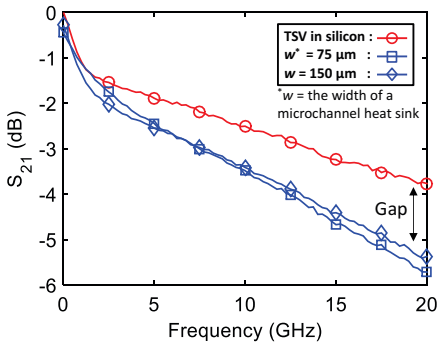

Fig. 10. Measurement results of insertion loss: TSVs in microchannel heat sink immersed in DI water and TSVs in a silicon substrate.

to the ground TSVs. As noted in Section II, the capacitive and conductive properties of DI water are higher than silicon at high frequencies. This indicates that the loss of microchannel-embedded TSVs (using DI water) is expected to be higher than TSVs in a silicon substrate. To analyze the frequency behavior of TSVs in terms of loss, two sets of TSVs in microchannels (microchannel widths of 75 µm and 150 µm) were characterized and compared to conventional TSVs in silicon, as shown in Fig. 10. At 20 GHz, the loss of TSVs in DI water shows an additional loss of ~2 dB, which is believed to be due to the high conductive property of DI

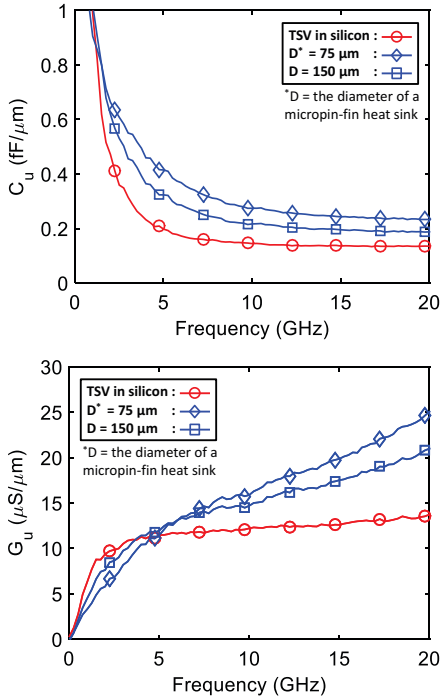

Fig. 11. Extracted p.u.l. capacitance (top) and conductance (bottom) from measurements: TSVs in microchannel heat sink immersed in DI water and TSVs in a silicon substrate

water at high frequencies. TSV loss further increases as the width of the microchannel decreases, or equivalently as the volume of DI water between signal and ground TSVs increases.

B. TSV Capacitance and Conductance Extraction of TSVs in a Micropin-fin Heat Sink

Using single-port characterization, the parasitics of TSVs embedded within the micropin-fins are extracted. The capacitance and conductance values are extracted using Y-parameters obtained from S-parameter measurements [19], [20]. Figure 11 illustrates the extracted per-unit-length (p.u.l.) TSV capacitance and conductance. Due to the high permittivity of DI water, the capacitance of TSVs increases as the diameter of the micropin-fin decreases, or equivalently, as the volume of DI water between TSVs increases. On the other hand, the conductance of TSVs initially decreases as the diameter of micropin-fin decreases. At 20 GHz, the total extracted capacitance of the TSVs is 0.23 fF/µm and 0.19 fF/µm when the diameter of the micropin-fins is 75 µm and 150 µm, respectively. These values correspond to a 64.3% and 35.7% increase in extracted TSV capacitance relative to TSVs in silicon. Similarly, the extracted conductance of the TSVs is 25.1 µS/µm and 21.0 µS/µm, respectively, which is 81.9 % and 52.2 % larger than in the silicon case. It is observed that as the volume of DI water between TSVs increases, the extracted capacitance and conductance of the TSVs increase at high frequencies.

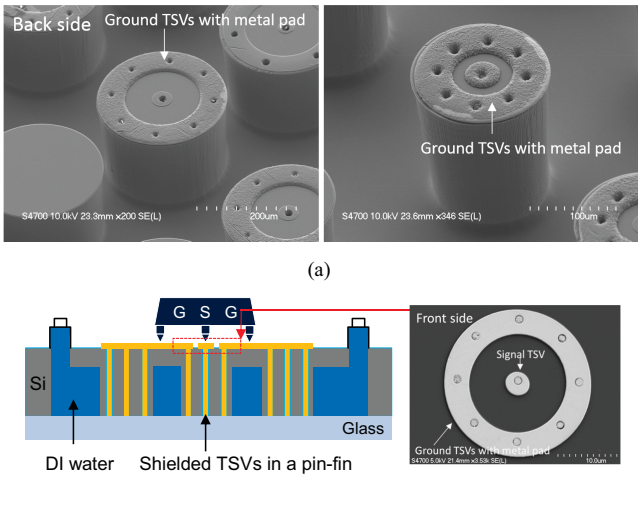

Fig. 12. (a) SEM images of coaxially shielded TSVs within a microfluidic pin-fin heat sink. TSV pitches of 100 µ m (left) and 50 µm (right) are shown. (b) Schematic of the measurement setup with an annular GSG pad that connects the ground TSVs.

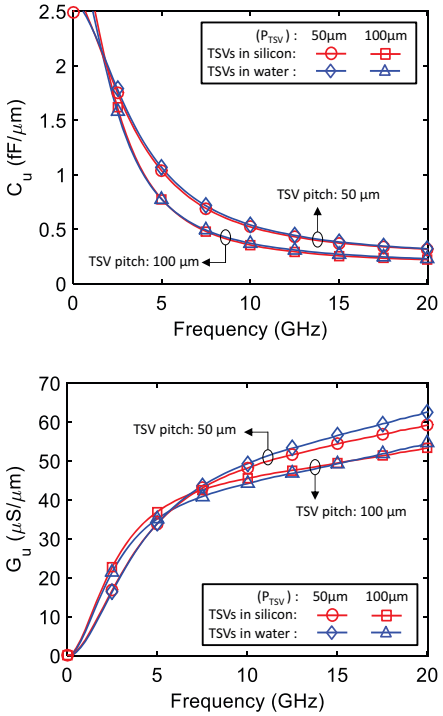

Fig. 13. Extracted p.u.l. capacitance (top) and conductance (bottom) from measurements of TSVs in silicon and TSVs in DI water. Two TSV pitches (100 µm and 50 µm) are shown in the plots.

C. Coaxially shielded TSVs in a Micropin-fin Heat Sink

In this section, we propose coaxially shielded TSVs whose electrical attributes are invariant to the coolant. Figure 12 illustrates a schematic and SEM images of microfluidic pin-fin-embedded coaxially shielded TSVs; a center-signal

TSV is surrounded by multiple ground TSVs, and an annular-shaped metal pad is used to connect the ground TSVs. Thus, the signal TSV can be largely shielded from the surrounding environment. Coaxially shielded TSVs of two TSV pitches (50 µm and 100 µm) with 8 ground TSVs in a microfluidic pin-fin heat sink are fabricated, as shown in Fig. 12 (a). Using the testbed in the Fig. 12 (b), the high-frequency characterization of the coaxially shielded TSVs is performed under two conditions; coaxially shielded TSVs within a silicon substrate and within a micropin-fin heat sink. Following the same Y-parameter conversion procedure as in the previous section, the extracted p.u.l. capacitance and conductance are plotted in Fig. 13. It should be noted that the extracted capacitance and conductance of the coaxially shielded TSVs in silicon and in DI water are highly consistent. Thus, the proposed coaxially shielded TSVs may have an important application in both high-speed digital as well as RF signaling.

V. CONCLUSION

This paper experimentally analyzes the impact of microfluidic cooling on the electrical performance of TSVs in 3-D ICs. The paper presents the design and fabrication of a testbed containing TSVs within two microfluidic heat sinks (micropin-fin and microchannel heat sinks) immersed in deionized (DI) water. The frequency response of TSVs in the testbed with DI water is characterized using a microprobe station and a network analyzer. Using the experimental testbed, the electrical characteristics of TSVs in a microfluidic heat sink are compared to conventional TSVs in silicon. Due to the high conductive property of DI water at high frequencies, TSVs in DI water show higher insertion loss, capacitance, and conductance than TSVs in silicon. Moreover, the paper demonstrates coaxially shielded TSVs embedded in a micropin-fin heat sink to electrically shield the signal TSVs from the surrounding DI water.

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